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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/769,591 | 01/30/2004 | Chidamber R. Kulkarni | X-1557-3 US | 8956 |

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| EXAMINER | |
|---|---|
| TO, TUYEN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/769,591 | KULKARNI ET AL. | |
| | Examiner | Art Unit | |
| | Tuyen To | 2825 | TT |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *9-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This is a response to the communication filed on 1/30/2004. **Claims 1-8 and 17-23** are pending. **Claims 9-16** are withdrawn.

### *Election/Restrictions*

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

**Group I, claims 1-8 and 17-23**, drawn to a method of designing a memory system for implementation with receiving specification data for generating a logical description and physical description of a memory system, classified in class 716, subclass 18.

**Group II, claims 9-16,** drawn to a design tool for designing a memory system for implementation with an input section for specifying attributes of a design memory system , a first database for storing a memory model, a second database for storing a physical memory configuration, and a memory model section for generating an instance of a design memory/ memory-interconnection and implementing the generated instances, classified in class 716, subclass 18.

2. The inventions are distinct, each from the other because of the following reasons: Inventions listed as Groups I-II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, inventions I-II have separate utility. Invention I discloses a method receives specification data of a memory system for generating a logical description of memory components and the physical description associated with the logical description. Invention II discloses a design tool

for attributes of a memory system and generates instances of memory components for implementation. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with **Kim Kanzaki (Reg. No. 37652)** on 04/04/2006 a provisional election was made **with traverse** to prosecute the invention of **Group I, claims 1-8 and 17-23**. Affirmation of this election must be made by applicant in replying to this Office action. **Claims 9-16** are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species or invention to be examined even though the requirement be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention or species may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse.

Should applicant traverse on the ground that the inventions or species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions or species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions

unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C.103(a) of the other invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

***Specification***

6. The disclosure is objected to because of the following informalities: on page 51, the title should not be included the abstract.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-5 and 17-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Horn et al. (Horn) (US Pub. No. 2003/0033374).

**Referring to claim 1 and similarly recited claim 17,** Horn discloses a method and apparatus of designing a memory system for using an integrated circuit, comprising:

receiving specification data including attributes of said memory system ( Figs. 10-12, element 422, paragraph [0054] );

generating a logical description of said memory system in response to said specification data (Figs. 10-12, element 424, paragraphs [0054]-[0055]), said logical description defining a memory component and a memory interconnection component ( paragraphs [0012]-[0014]); and

generating a physical description of said memory system in response to said logical description (Figs. 10-12, elements 426 and 428, paragraphs [0054]-[0055]), said physical description including memory circuitry associated with said integrated circuit defined by said memory component, said memory circuitry having an interconnection topology (paragraphs [0011], [0040], and [0042] )defined by said memory interconnection component (paragraphs [0012]-[0014] and [0011]).

**Referring to claim 2 and similarly recited claim 18**, Horn discloses the method of claim 1 and apparatus of claim 17 respectively, further comprising:

defining said specification data using a set of primitives configured to generate descriptions for said memory system attributes (paragraph [0055]).

**Referring to claim 3**, the method of claim 2, wherein said set of primitives comprises extensible markup language (XML) constructs (applicants admitted XML is a standardized format and is well-known in the art, see specification on page 35).

**Referring to claim 4 and similarly recited claim 19**, Horn discloses the method of claim 1 and apparatus of claim 17 respectively, wherein said memory circuitry is disposed within said integrated circuit (Figs. 4 and 6; paragraph [0013]).

**Referring to claim 5 and similarly recited claim 20**, Horn discloses the method of claim 1 and apparatus of claim 17 respectively, wherein a portion of said memory circuitry is disposed within said integrated circuit, and a remaining portion of said memory circuitry is disposed external to said integrated circuit (Figs. 2 and 4, paragraph [0043].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 6-7 and 21-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn et al. (Horn) in view of Katayama et al (Katayama)(US Patent No. 5,867,180).

**Referring Claims 6 and similarly recited claim 21,** Horn discloses the method of claim 1 and apparatus of claim 17 respectively, *except* wherein said memory component is defined by a memory architecture and a memory interface, and wherein said memory interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface.

Katayama discloses wherein said memory component is defined by a memory architecture and a memory interface, and wherein said memory interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface (Figs 6-8, col. 5, line 8 to col. 6, line 32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the methods of Horn with the method disclosed by Katayama because such combined method would provide an improved memory system with flexible configurations of the multiple frame buffers (Katayama, col. 2, lines 4-6).

**Referring to claim 7 and similarly recited claim 22**, the method of claim 6 and apparatus of claim 21 respectively, wherein said memory system is configured to store messages (Horn, Figs. 2-4, paragraph [0042]-[0044], see instruction and data buffer 118 and data memory 148), wherein said memory circuitry comprises a single memory (Horn, Figs. 2-4, paragraph [0042]-[0044], see data memory 148), and wherein said memory architecture is configured to store all of said messages in said single memory (Horn, Figs. 2-4, paragraph [0042]-[0044], see data memory 148).

9. **Claims 8 and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn et al. (Horn) in view of Katayama et al. (Katayama) and in further view of Utas (US Patent No. 6647431).

**Referring to claim 8 and similarly recited claim 23**, Horn and Katayama disclose the limitations of claims 6 and 21 from which claims 8 and 23 depend respectively.

Horn and Katayama do not disclose wherein said memory system is configured to store messages, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories.

Utas disclose wherein said memory system is configured to store messages, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories (Utas, Fig. 2, col. 2, line 34 to col. 5, line16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the methods of Horn and Katayama with the method disclosed by Utas because such combined method includes a memory system having a plural of memories configured to store messages would provide an efficient method for handling input/output messages for plural call processing applications which reside on a processor subsystem of a mobile switch center (Utas, see abstract, col. 1, lines 42-55).

***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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